ADM-PCIE-8K5
User Manual

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1 Introduction

The ADM-PCIE-8K5 is a high-performance reconfigurable computing card intended for Data Center applications, featuring a Xilinx Kintex UltraScale FPGA.

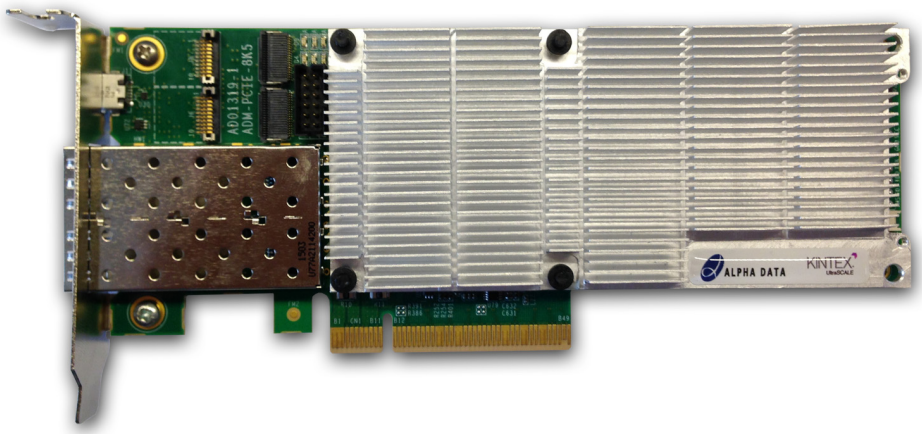

Figure 1 : ADM-PCIE-8K5 Product Photo

1.1 Key Features

Key Features

- PCIe Gen1/2/3 x1/2/4/8 capable
- Half-length, low-profile x8 PCIe form factor
- Two banks of DDR4 SDRAM 72 bit wide memory (ECC), 16GB (8GB per bank) default rated at 2400MT/s, 32GB option rated at 1866MT/s.
- Two SFP+ sites capable of data rates up to 16.375 Gbps per channel
- Two Samtec FireFly sites capable of data rates up to 16.375 Gbps per channel (65.5 Gbps per module). Can be routed to front panel or adjacent card slots.
- Optional SMA/U.FL timing input
- Front Panel JTAG Access via USB port
- FPGA configurable over USB/JTAG and BPI configuration flash
- XCKU115-2FLVA1517E FPGA
- Voltage, current, and temperature monitoring

1.2 Order Code

ADM-PCIE-8K5(m)(s)(g)(j)

See http://www.alpha-data.com/pdfs/adm-pcie-8k5.pdf for complete ordering options.

2 PCB Information

2.1 Physical Specifications

The ADM-PCIE-8K5 complies with PCI Express CEM revision 3.0.

Description	Measure
PCB Dy	64.4 mm
PCB Dx	167.65 mm
PCB Dz	1.6 mm

Table 1 : Mechanical Dimensions (PCB only)

Description	Measure
Total Dy	68.9 mm
Total Dx (Inc. SFP+ Cages)	173 mm
Total Dz	17.5 mm
Weight	200g

Table 2 : Mechanical Dimensions

2.2 Chassis Requirements

2.2.1 PCI Express

The ADM-PCIE-8K5 is capable of PCIe Gen 1/2/3 with 1/2/4/8 lanes, using the Xilinx Integrated Block for PCI Express.

2.2.2 Mechanical Requirements

An 8-lane or 16-lane physical PCIe slot is required for mechanical compatibility.

Each ADM-PCIE-8K5 is shipped with a full height PCIe card bracket installed by default. A half-height bracket is shipped along with the product and can be easily changed out with a philips screw driver. If the application requires a low-profile bracket and the order quantity is high, contact sales@alpha-data.com to get the correct bracket fitted before shipping.

2.2.3 Power Requirements

The PCIe Specification permits a standard low-profile, half-length PCIe card to dissipate up to 25 W of power, drawn from the PCIe slot. The ADM-PCIE-8K5 may consume more than 25 W of power for larger user FPGA designs. Power estimation requires the use of the Xilinx XPE spreadsheet and/or a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.95	VCC_INT + VCCINT_IO + VCC_BRAM	36A
1.8	VCCAUX + VCCAUX_IO VCCO_1.8V	3A
3.3	VCCO_3.3V	2A
1.2	VCCO_1.2V	20A
1.8	MGTVCCAUX	1A
1.0	MGTAVCC	5A
1.2	MGTAVTT	2A

Table 3 : Available Power By Rail

2.3 Thermal Performance

The ADM-PCIE-8K5 comes with a heat sink to reduce the heat of the FPGA which is typically the hottest point on the card. The FPGA die temperature must remain under 100 degrees Celsius or the system monitor will clear the FPGA design to ensure the card does not overheat. To calculate the FPGA die temperature, take your application power and multiply by Theta JA from the table below, and add your systems internal ambient temperature. If you are using the fan provided with the board, you will find Theta JA is approximately 1.6 degC/W for the board.

The power dissipation can be estimated by using the Alpha Data power estimator in conjuction with the Xilinx Power Estimator (XPE) downloadable at http://www.xilinx.com/products/technology/power/xpe.html. Download the UltraScale tool and set the Device to Kintex UltraScale, KU115, FLVA1517, -2, Extended. Set the ambient temperature to your system ambient and select User Override for the Effective theta JA and enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next aquire the 8K5 power estimator from Alpha Data by contacting support@alpha-data.com. You will then plug in the FPGA power figures along with DDR4 and SFP usage to get an estimated board level power dissipation.

The graph below shows Theta JA of the board with two 3.5 watt QSFP loopback connectors inserted.

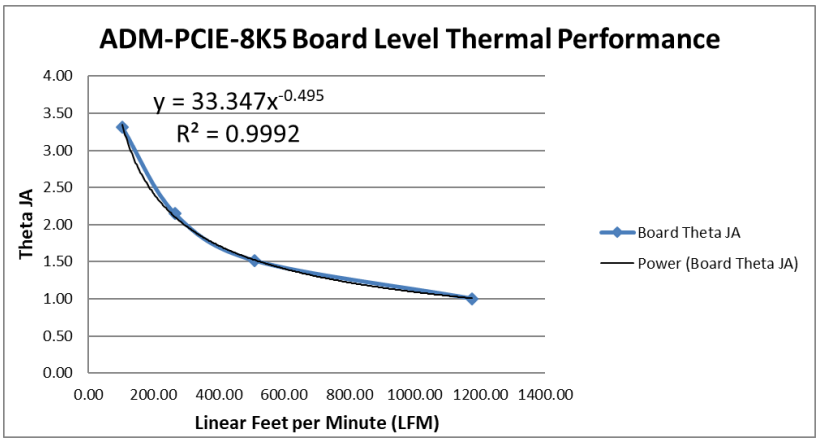

Figure 2 : Thermal Performance

2.4 Optional Blower

Because it is possible for generic PC chassis to not provide sufficient airflow to cool the FPGA, the ADM-PCIE-8K5 is shipped with an uninstalled blower. The blower is optional and can be easily installed with a Philips screw driver at the discretion of the user. Before screwing in the blower, plug in the small power connector into the right angle connector along the back edge of the board. The blower hangs off the back of the PCB outside of the PCIe card envelope.

Figure 3 : Thermal Performance

3 Functional Description

3.1 Overview

The ADM-PCIE-8K5 is a versatile reconfigurable computing platform with a Kintex UltraScale KU115-2E FPGA, Gen3x8 PCIe interface, two banks of DDR4 both 72 bits wide (for 64 bits with 8 bits ECC), two SFP+ cages capable of up to 16.375Gbps each and any Xilinx supported standard (Ethernet, SRIO, Infiniband, SDI, etc.), two Samtec FireFly connectors also capable of 16.375G/channel (8 channels), a U.FL input for a timing synchronization input, a 12 pin header for general purpose use (clocking, control pins, debug, etc.) and low speed serial communications, and a robust system monitor.

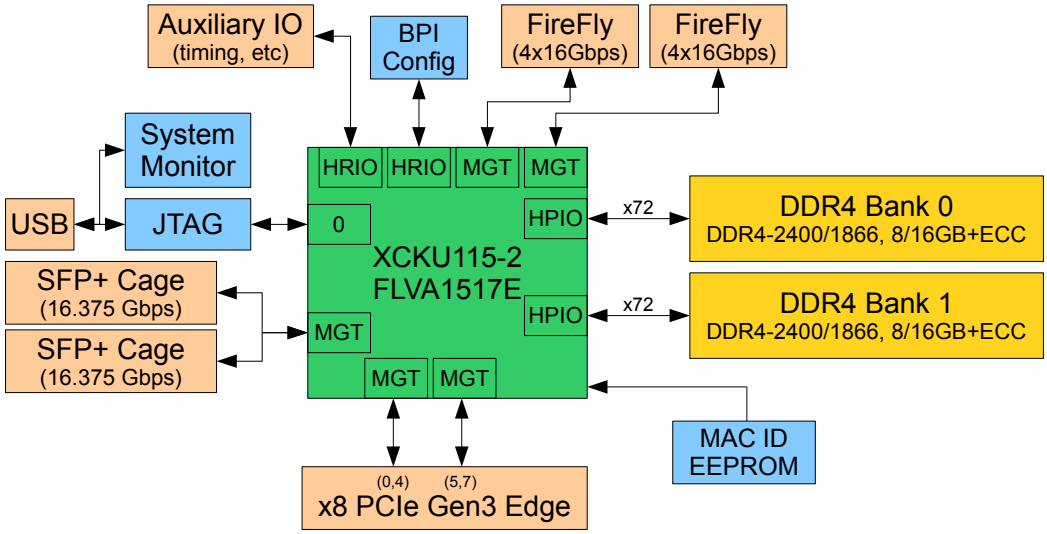

Figure 4 : ADM-PCIE-8K5 Block Diagram

3.1.1 Switches

The ADM-PCIE-8K5 has a quad DIP switch SW1, located on the rear side of the board. The function of each switch in SW1 is detailed below:

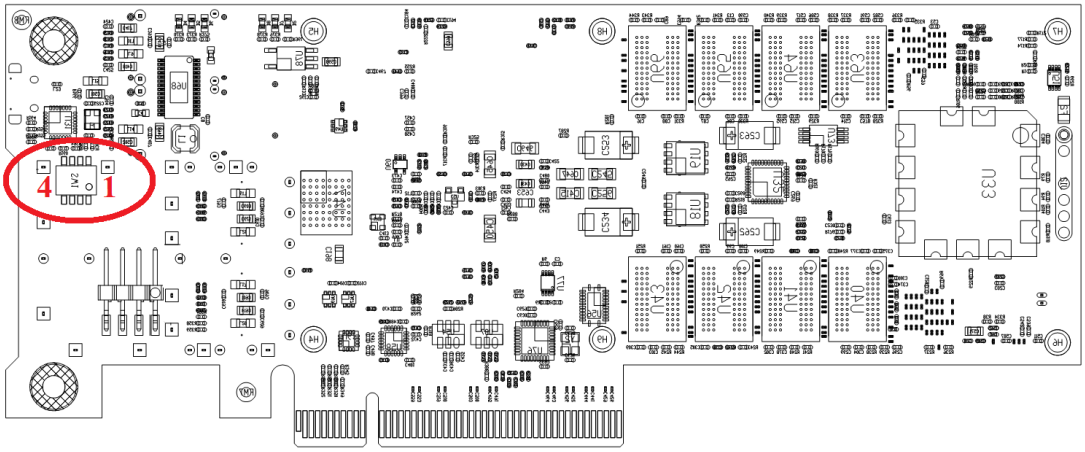

Figure 5 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	User Switch	Pin AV18 = '1'	Pin AV18 = '0'
SW1-2	OFF	Flash Lockdown/ PCIe I2C Isolation	Flash block Lockdown enabled/ PCIe I2C isolated	Flash block Lockdown disabled/ PCIe I2C connected to system monitor
SW1-3	OFF	Service Mode	Regular Operation	Firmware update service mode
SW1-4	OFF	PCIe Edge JTAG	JTAG to FPGA from USB	JTAG to FPGA from PCIe Edge

Table 4 : SW1 Switch Functions

SW1-2 PCIe I2C isolation feature is not implemented in Rev3 and earlier (serial number less than 1300).

Use IO Standard "LVCMOS33" when constraining the user switch pin.

3.1.2 LEDs

There are 6 LEDs on the ADM-PCIE-8K5, 3 of which are general purpose and whose meaning can be defined by the user. The other four have fixed functions described below:

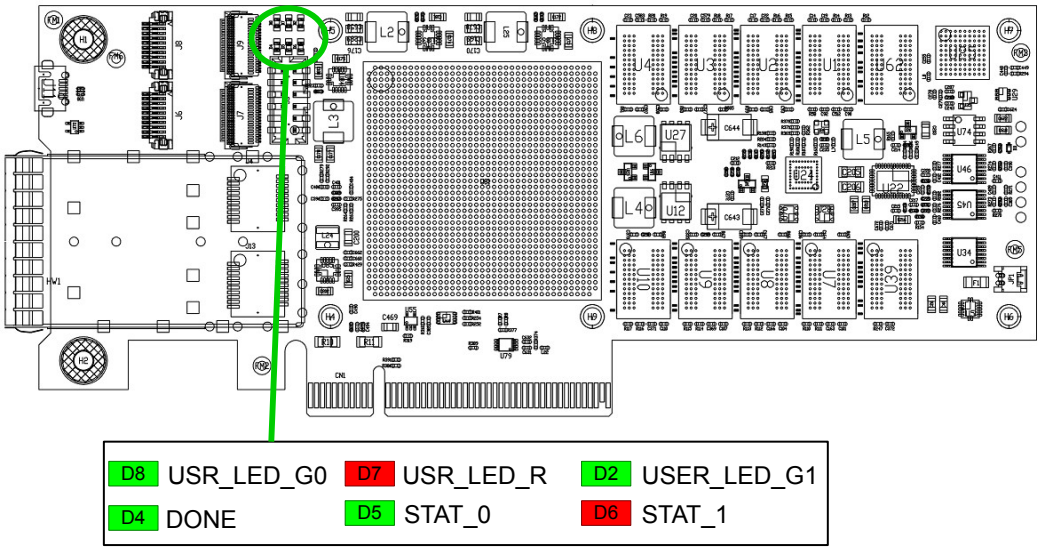

Figure 6 : LEDs

Comp. Ref.	Function	ON State	OFF State
D4	DONE	FPGA is configured	FPGA is not configured
D2	USER_LED_G0	User defined '0' pin AT19	User defined '1' pin AT19
D8	USER_LED_G1	User defined '0' pin AU19	User defined '1' pin AU19
D7	USER_LED_R	User defined '0' pin AU20	User defined '1' pin AU20
D5	Status 0	See Status LED Definitions	
D6	Status 1	See Status LED Definitions	

Table 5 : LED Details

Use IO Standard "LVCMOS33" when driving the user LED pins.

3.2 Clocking

The ADM-PCIE-8K5 provides reference clocks for the DDR4 SDRAM banks and the I/O interfaces available to the user. After a clock is programmed to a certain frequency, that frequency will become the default on power-up. Any clock out of an Si5338 Clock Synthesizer is re-configurable over I2C. This allows the user to configure almost any arbitrary clock frequencies during application run time. Please see the Alpha Data AVR2Util application and API functions for details. Maximum programable clock frequency is 312.5MHz

Note: use "set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]" to ensure the user design does not interfere with the I2C interface to the reprogramable clock generator.

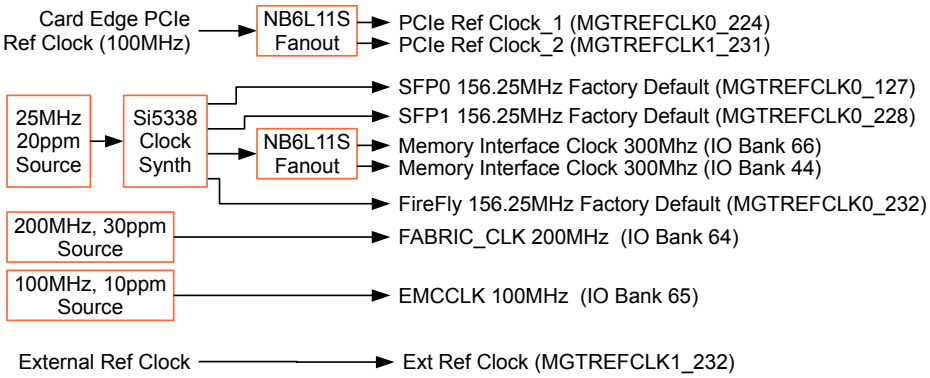

Figure 7 : Clock Topology

3.2.1 PCIe Reference Clocks

The 8 MGT lanes connected to the PCIe card edge use MGT tiles 224/225 and use the system 100 MHz clock (PCIE_REFCLK).

A second PCIe reference clock is buffered up from the edge to the FireFly module MGT tiles (231/232).

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
PCIE_REFCLK_1	MGTREFCLK1_231	LVDS	H10	H9
PCIE_REFCLK_2	MGTREFCLK0_224	LVDS	AT10	AT9

Table 6 : PCIe Reference Clocks

3.2.2 Fabric Clock

The design offers a fabric clock called FABRIC_CLK which is permanently fixed at 200 MHz. This clock is intended to be used for IDELAY elements in FPGA designs. The fabric clock is connected to a Global Clock (GC) pin.

Signal	Target FPGA Input	I/O Standard	pin
FABRIC_CLK	IO_L12P_T1U_GC_64	LVCMOS33	AM19

Table 7 : Fabric Clock

3.2.3 Programming Clock (EMCCLK)

An 100MHz clock is fed into the EMCCLK pin to drive the BPI flash device during configuration of the FPGA.

Signal	Target FPGA Input	I/O Standard	pin
REFCLK100M	IO_L24P_T3U_N10_EMCCLK_65	LVCMOS18	AJ28

Table 8 : EMCCLK

3.2.4 SFP+

The SFP+ cages are located in MGT tiles 227 and 228 and use two unique clock sources. Both clocks are initially set to 156.25MHz. Note that these clock frequency can be changed to any arbitrary clock frequency up to 400MHz by re-programing the Si5338 reprogrammable clock oscillator via system monitor. This can be done using the Alpha Data API or over USB with the appropriate Alpha Data Software tools. Any changes made to the default clock frequency are non-volatile and will be used moving forward.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
GTH_CLK_0	MGTREFCLK0_227	LVDS	AE8	AE7
GTH_CLK_1	MGTREFCLK0_228	LVDS	AA8	AA7
SI5328_REFCLK_OUT0	MGTREFCLK1_228	LVDS	W8	W7

Table 9 : SFP+ Reference Clocks

The SFP+ cages are also located such that they can be clocked from a Si5328 jitter attenuator clock multiplier. If jitter attenuation is required please see the reference documentation for the Si5328. https://www.silabs.com/Support%20Documents/TechnicalDocs/Si5328.pdf

The Si5328 is configured with a 114.285MHz oscilator on XA and XB, SDA and SCL pins can be found in the Complete Pinout Table at net names SI5328_1V8_SCL and SI5328_1V8_SDA (external pull-ups included).

The Si5328 input clock comes from FPGA pins found in the Complete Pinout Table at net names SI5328_REFCLK_IN_P/N, and includes 100 Ohm AC coupled termination on the 1.8V FPGA bank.

The Jitter Attenuator is not fitted on rev3 and earlier (serial number less than 1300)

3.2.5 FireFly

The two FireFly sites are located in MGT tile 231 and 232 and can use a variety of reference clocks.

PCIE_REFCLK_1 is a buffered version of the PCIe edge clock. It is converted to LVDS through a NB6L11S clock buffer.

GTH_CLK_2 is default to 156.25MHz. Note that these clock frequency can be changed to any arbitrary clock frequency up to 400MHz by re-programing the Si5338 reprogrammable clock oscillator via system monitor. This can be done using the Alpha Data API or over USB with the appropriate Alpha Data Software tools. Any changes made to the default clock frequency are non-volatile and will be used moving forward.

EXT_CLK comes from the GPIO header. The signal is fed directly to the GTH clock with only 10nF capacitors in series. Take care to supply a safe clock in on these signals. See Xilinx UG576 for more details acceptable on GTH reference clocks.

SI5328_REFCLK_OUT1 comes from the onboard jitter attenuator which can feedback a recovered clock from the GTH channel for particular standards. The Jitter Attenuator is not fitted by default and requires a custom bulid option. Contact sales@alpha-data.com for more details.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
SI5328_REFCLK_OUT1	MGTREFCLK0_231	LVDS	K10	K9
PCIE_REFCLK_1	MGTREFCLK1_231	LVDS	H10	H9
GTH_CLK_2	MGTREFCLK0_232	LVDS	F10	F9
EXT_CLK	MGTREFCLK1_232	User	D10	D9

Table 10 : FireFly Reference Clocks

3.2.6 DDR4 SDRAM Reference Clocks

The two banks of DDR4 SDRAM memory each require a separate reference clock, as per Xilinx UltraScale MIG design guidelines. The reference clocks for these interfaces are detailed below:

Both clocks are 300MHz by default.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
MEM_CLK_0	IO_L11_T1U_GC_66	DIFF_HSTL_I_12 (or SSTL)	G16	G15
MEM_CLK_1	IO_L11_T1U_GC_44	DIFF_HSTL_I_12 (or SSTL)	AM22	AN22

Table 11 : Memory Reference Clocks

3.3 PCI Express

The ADM-PCIE-8K5 is capable of PCIe Gen 1/2/3 with 1/2/4/8 lanes. The FPGA drives these lanes directly using the Integrated PCI Express block from Xilinx. Negotiation of PCIe link speed and number of lanes used is generally automatic and does not require user intervention.

PCI Express reset (PERST#) connected to the FPGA at both pins AE15 and AM15.

The other pin assignments for the high speed lanes are provided in the pinout attached to the Complete Pinout Table

Note:
Different motherboards/backplanes will benefit from different RX equalization schemes within the PCIe IP core provided by Xilinx. Alpha Data recommends using the following setting if a user experiences link errors or training issues with their system: within the IP core generator, change the mode to "Advanced" and open the "GT Settings" tab, change the "form factor driven insertion loss adjustment" from "Add-in Card" to "Chip-to-Chip" (See Xilinx PG239 for more details).

3.4 DDR4 SDRAM

Two banks of DDR4 SDRAM memory are soldered down to the board. While the factory default is 8GB/per bank, 16GB/bank is also supported through a build variant. Please see Order Code for all order options. The memory interface is 72-bit wide data (64 data + 8 ECC). Maximum signaling rate is 2400 MT/s for 16GB total and 1688MT/s with 32GB total.

Memory solutions are available from the Xilinx Memory Interface Generator (MIG) and must use Vivado 2016.1 or later. An example project with traffic generator is available with purchase of the ADM-PCIE-8K5 SDK. However, all the information required to generate a complete MIG IP core is available within this user guide.

3.4.1 MIG IP setup requirements for rev 1 PCBs

8GB per bank, rev1 PCB

- Vivado 2016.1 IP Catalog: DDR4 SDRAM (MIG)
- Memory Device Interface Speed (ps): 938
- Refernce Input Clock speed (ps): 3332
- Custom Parts Data File: Checked, use 'adm-pcie-8k5_custom_parts_2133.csv' downloaded from www.alpha-data.com/8k5
- Configuration: Components
- Memory Part: CUSTOM_DBI_MT40A1G8PM-083E
- Data Mask and DBI: NO DM DBI WR RD
- IO locations found in appendix

3.4.2 MIG IP setup requirements rev2 + newer PCBs

8GB per bank, rev2 and newer PCB

- Vivado 2016.3 IP Catalog: DDR4 SDRAM (MIG)
- Memory Device Interface Speed (ps): 833
- Refernce Input Clock speed (ps): 3332
- Custom Parts Data File: Checked, use 'adm-pcie-'8k5_custom_parts_2400.csv' downloaded from www.alpha-data.com/8k5
- Configuration: Components
- Memory Part: CUSTOM_DBI_MT40A1G8PM-083E
- Data Mask and DBI: NO DM DBI WR RD
- IO locations found in appendix

3.5 SFP+

Two SFP+ cages are available at the front panel. Both cages are capable of housing either active optical or passive copper SFP compatible components. The communication interface can run at up to 16.375Gbps per channel. These cages are ideally suited for 10 Gigabit Ethernet or any other protocol supported by the Xilinx GTH Transceivers. Please see Xilinx User Guide UG576 for more details on the capabilities of the transceivers.

Both SFP+ cages have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is SFP0 and SFP1 with locations clarified in the diagram below.

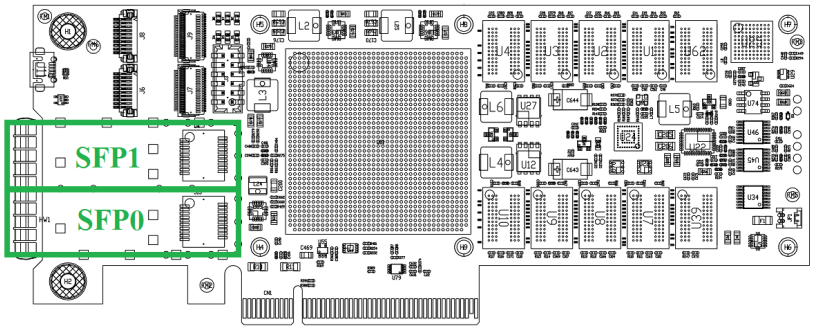

Figure 8 : SFP Locations

3.6 FireFly

Two FireFly receptacles near the front of the board allow for additional 16.375G lanes. The FireFly connections have the same capabilities as the SFP+ cages, with much greater lane width. There are 4 lanes per FireFly, adding up to 8 lanes at 16.375Gps resulting in 131Gbps total bandwidth. This can be configured in a ring orientation as depicted in the image below, or allow for MPO style breakouts at the front panel (full-height panel only).The ADM-PCIE-8K5 support both copper and optical FireFly modules. More information on FireFly can be found at https://www.samtec.com/optics/optical-cable/mid-board/firefly

Both FireFly sites have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is FireFly0 and FireFly1 with locations clarified in the diagram below.

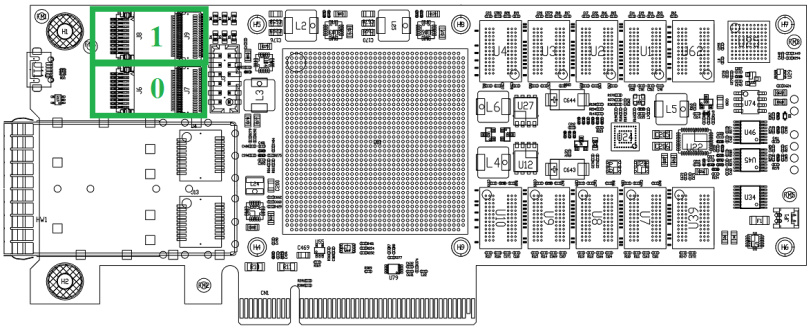

Figure 9 : FireFly Locations

The FireFly modules may be connected between adjacent ADM-PCIE-8K5 boards in order to form powerful distributed processing rings.

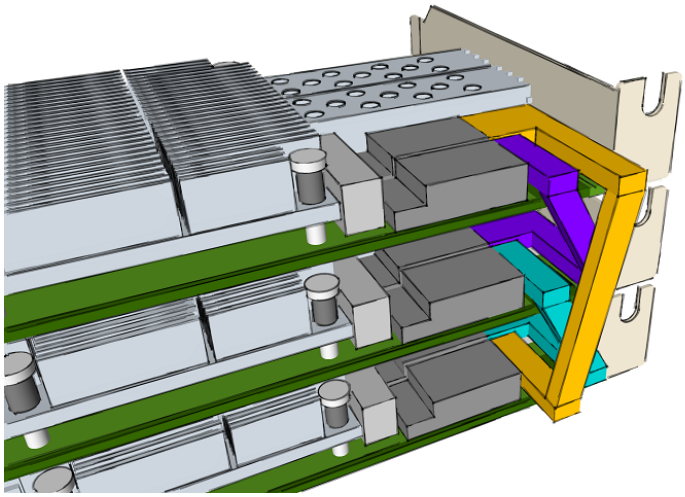

Figure 10 : FireFly Ring Connections

The FireFly modules are broken out to the front panel as shown in the image below. The Samtec FireFly optical module ties the PCB to the front panel where an industry standard MPO coupler is used for attachment to external cabling.

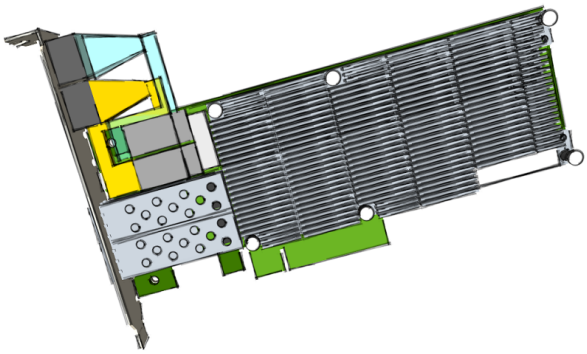

Figure 11 : FireFly Breakout to Front Panel

The FireFly sites can fit a number of standard cables. Below is a list of supported part numbers. Contact Alpha Data or your local Samtec representative for more details.

Description	Part Number	Manufacturer
56G/40G (4x14/10) FireFly Optical Transceiver	ECUO B04 14 017 0 2 1 1 01	Samtec
65.5G (4x16.375) FireFly Copper Cable	ECUE 08 020 T2 FF B4 1 D1	Samtec

Table 12 : FireFly Part Numbers

3.7 System Monitor

The ADM-PCIE-8K5 monitors temperature, voltage, and current of the board to check on the operation of the board. The monitoring is implemented using an Atmel AVR microcontroller. All readings and measurements are available to the FPGA, enabling detailed power consumption reporting.

Control algorithms within the microcontroller automatically check line voltages and on board temperatures and shares makes the information available to the FPGA over a dedicated serial interface built into the Alpha Data reference design package (sold separately). The information can also be accessed directly from the microcontroller over the USB interface on the front panel or via the IPMI interface available at the PCIe card edge.

Index	Monitors	Purpose/Description
ADC00	12.0V	Board Input Supply
ADC01	3.3V	Board Input Supply
ADC02	3.3V	Board Input Auxilary Power Supply
ADC03	3.3V	Internally generated supply
ADC04	2.5V	Clock Voltage Supply
ADC05	1.8V	FPGA IO Voltage (VCCO)
ADC06	1.8V	Transceiver Power (AVCC_AUX)
ADC07	1.2V	DDR4 SDRAM and FPGA memory I/O
ADC08	1.2V	Transceiver Power (AVTT)
ADC09	1.0V	Transceiver Power (AVCC)
ADC10	0.95V	FPGA Core Supply (VccINT)
ADC11	0.6V	DDR4 Termination Voltage
ADC12	12V_I	12V input current in amps
ADC13	3.3V_I	3.3V input current in amps
TMP00	uC	Micro-controller on-die temperature
TMP01	Board	temperature sensor on PCB
TMP02	NC	Not Connected
TMP03	FPGA	FPGA on-die temperature

Table 13 : Voltage, Current, and Temperature Monitors

Note:
The current measurement results returned on rev3 and earlier PCBs are scaled incorrectly. Please divide each current measurement by a factor of 1.5 to improve accuracy.

3.7.1 Automatic Temperature Monitoring

Automatic over-temperature shutdown was added as a function external to the FPGA from sn409 and onwards. The over-temperature shutdown function will clear the FPGA program if the die temperature exceeds 100 degrees Celsius.

3.7.2 System Monitor Status LEDs

LEDs D6 (Red) and D5 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 14 : Status LED Definitions

3.8 SMA Timing Input

All cards are fitted with a U.FL connector that can be utilized as a timing input. This connector can be accessed with a U.FL cable internal to the chassis, or cabled to an SMA or similar connector at the frton panel. Contact sales@alpha-data.com for front panel connector options.

Input is on FPGA pin AL30, IOSTANDARD LVCMOS18

The signal is isolated through a optical isolator part number ACPL-M61L with a 739 ohm of series resistance.

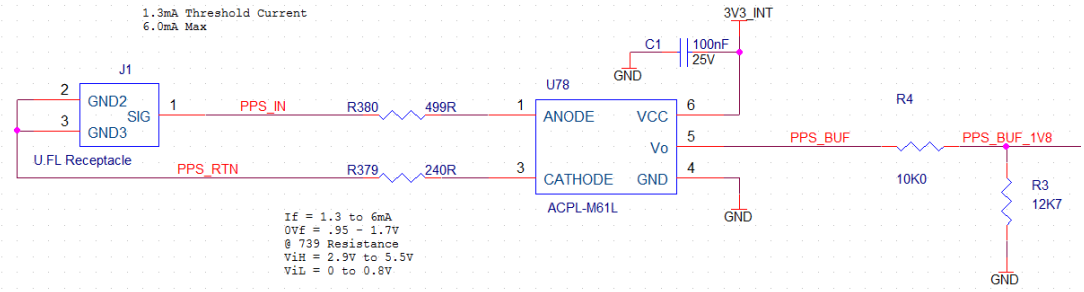

Figure 12 : Timing Input Schematic

3.9 USB Front Panel Interface

For convenience the FPGA can be configured directly from the USB connection on the front panel. The ADM-PCIE-8K5 utilizes the Digilent USB-JTAG converter box which is supported by the Xilinx software tool suite. Simply connect a micro-USB AB type cable between the ADM-PCIE-8K5 USB port and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the FPGA and allow you to configure the FPGA and the BPI configuration PROM.

The same USB connector is used to directly access the system monitor system. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/windows
https://support.alpha-data.com/pub/firmware/utilities/linux

Use "avr2util.exe /?" to see all options.

For example "avr2util.exe /usbcom com4 display-sensors" will desiplay all sensor values.

For example "avr2util.exe /usbcom com4 setclknv 0 100000000" will set the GTH_CLK_0 100MHz.
Index 0: GTH_CLK_0
Index 1: GTH_CLK_1
Index 2: MEM_CLK
Index 3: GTH_CLK_2

Change 'com4' to match the com port number assigned under windows device manager.

3.10 Configuration

There are two main ways of configuring the FPGA on the ADM-PCIE-8K5:

- From Flash memory, at power-on, as described in Section 3.10.1
- Using USB cable connected at the front panel USB port Section 3.10.2

3.10.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from a 1 Gbit BPI flash memory device (Micron part number MT28GU01GAAA1EGC-0SIT). This Flash device is divided into two regions of 64 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a KU115 FPGA.

The ADM-PCIE-8K5 is shipped with a bitstream, corresponding to the "dma_demo" FPGA design from the ADM-PCIE-8K5 SDK, programmed into region 1 and "reg_access" programmed into region 0. This permits basic confidence and performance testing to be performed on a board without needing to program anything into the Flash memory. Alpha Data recommends that region 0 is used as a fallback image; this permits relatively simple recovery, without requiring direct programming of the FPGA over the front panel USB connection, in the event of programming a "bad" bitstream into region 1.

The flash address map is as detailed below:

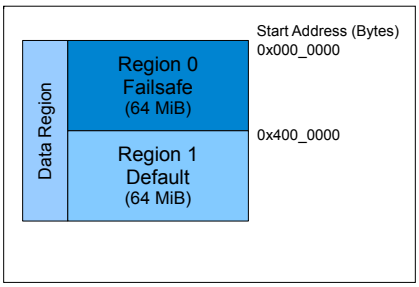

Figure 13 : Flash Address Map

At power-on, the FPGA attempts to configure itself automatically in BPI mode from region 1 unless the configuration header on the bitstream ultilizes multi-boot. Multibook and ICAP can be used to selected between the two configuration regions to be loaded into the FPGA. See Xilinx UG570 MultiBoot for details.

The Lockdown function of the Flash device is controlled via switch SW1-2. When SW1-2 is OFF, any blocks in the Flash whose Lockdown flag is set are write-protected. The factory default for the Lockdown flag of all Flash blocks is clear, so that any block in the Flash can be written.

3.10.1.1 Building and Programming Configuration Images

Generate a bitfile with these constraints (see XAPP587):

- set_property BITSTREAM.GENERAL.COMPRESS {TRUE} [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.BPI_SYNC_MODE {TYPE1} [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property BITSTREAM.CONFIG.OVERTEMPSHUTDOWN Enable [current_design]
- set_property CONFIG_MODE {BPI16} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 128
- -interface BPIx16

- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (failsafe location)
- -loadbit "up 0x2000000 <directory/to/file/filename.bit>" (default location)

Program with vivado hardware manager with these settings:

- BPI part number: mt28gu01gaax1e-bpi-x16
- State of non-config mem I/O pins: Pull-none
- RS bits: 25:24

3.10.1.2 Custom Flash Write Interface

Alpha Data's reference design bridge allows users to write images to the BPI configuration flash over the PCIE interface. Other customers may want similar functionality built into their own IP. In order to enable this functionality, users must reference the FLASH* pins in Complete Pinout Table and utilize the STARTUPE3 primitive to control certain dedicated configuration pins (i.e. D0-D3). Complete details on the STARTUPE3 primitive can be found in Xilinx UG570.

3.10.2 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel USB port. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager via the integrated Digilent JTAG converter module.

3.11 GPIO

The ADM-PCIE-8K5 has a GPIO feature. This feature is partially fit by default, and if serial transceivers are required it must be specified in the part number. See Order Code for more details on ordering options.

The GPIO interface consists of a versatile shrouded connector from Molex with part number 0878331220 that give users with custom IO requirements multiple connectivity options. The connector houses two types of signal, direct connect to FPGA signals (always present) and low speed serial communication signals (optional).

Recommended mating plug: Molex 0875681273

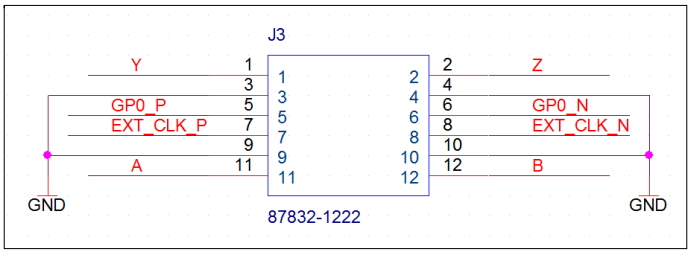

Figure 14 : GPIO Connector

3.11.1 Direct Connect FPGA Signals

Four nets are broken out to the GPIO header as two differential pairs. The first pair, is called GP0 and these signal are suitable for any 1.8V supported signaling standards supported by the Xilinx UltraScale architecture. See Xilinx UG571 for IO options. LVDS and 1.8 CMOS are popular options. The second pair is EXT_CLK, which is a differential pair that is routed directly to a GTH clock input. This can be used to either clock the FireFly GTH tiles, or as a global clock used anywhere in the design.

The direct connect GP0 signals are limited to 1.8V by a quickswitch (74CBTLVD3861BQ) in order to protect the FPGA from overvoltage on IO pins. This quickswitch allows the signals to travel in either direction with only 4 ohms of series impedance and less than 1ns of propagation delay. The nets are directly connected to the FPGA after the quickswitch.

Direct connect signal names are labeled GP0_1V8_P/N and EXT_CLK_P/N to show polarity and grouping. The signal pin allocations can be found in Complete Pinout Table

This header is always populated on the board and these signal are always available.

3.11.2 Low Speed Serial IO

A pin configurable serial buffer transceiver allows for RS232, RS485, and RS422 signal standard support. For details on configuring the transceiver please reference the IC manufacturer datasheet. Linear Technologies part number LTC2870. Direct link: http://cds.linear.com/docs/en/datasheet/28701fa.pdf

Signal naming is kept consistent with the Linear Tech datasheet and FPGA pin allocations can be found in the Complete Pinout Table. Be sure to constrain and drive each control pin for expected behavior.

This device is not normally fitted. Please see the order options if you require RS232/485 signaling standards.

3.12 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number M24C02-RMC6TG.

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP, SPARE_SCL, and SPARE_SDA respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

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Appendix A: Complete Pinout Table

Pin Number	Signal Name	Bank Voltage
U9	1V8_DIG	INPUT
AT18	AVR_B2U	3.3
AU16	AVR_HS_B2U	3.3
AU17	AVR_HS_CLK	3.3
AV19	AVR_HS_U2B	3.3
AW18	AVR_MON_CLK	3.3
AT17	AVR_U2B	3.3
AC11	CCLK	1.8
D14	DDR4_0_A0	1.2
F15	DDR4_0_A1	1.2
C14	DDR4_0_A10	1.2
E12	DDR4_0_A11	1.2
B14	DDR4_0_A12	1.2
J15	DDR4_0_A13	1.2
H12	DDR4_0_A14	1.2
B16	DDR4_0_A15	1.2
A15	DDR4_0_A16	1.2
L13	DDR4_0_A17	1.2
G12	DDR4_0_A2	1.2
E13	DDR4_0_A3	1.2
A13	DDR4_0_A4	1.2
C12	DDR4_0_A5	1.2
B12	DDR4_0_A6	1.2
F12	DDR4_0_A7	1.2
D13	DDR4_0_A8	1.2
C13	DDR4_0_A9	1.2
F13	DDR4_0_ACT_N	1.2
A12	DDR4_0_ALERT_N	1.2
B15	DDR4_0_BA0	1.2
F14	DDR4_0_BA1	1.2
G14	DDR4_0_BG0	1.2
H14	DDR4_0_BG1	1.2
L12	DDR4_0_C0	1.2

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
E15	DDR4_0_C1	1.2
J13	DDR4_0_C2	1.2
K12	DDR4_0_CK_C	1.2
K13	DDR4_0_CK_T	1.2
E16	DDR4_0_CKE	1.2
D15	DDR4_0_CS_N	1.2
D19	DDR4_0_DM0	1.2
D24	DDR4_0_DM1	1.2
L17	DDR4_0_DM2	1.2
T23	DDR4_0_DM3	1.2
H19	DDR4_0_DM4	1.2
H21	DDR4_0_DM5	1.2
K21	DDR4_0_DM6	1.2
P19	DDR4_0_DM7	1.2
P13	DDR4_0_DM8	1.2
B20	DDR4_0_DQ0	1.2
C18	DDR4_0_DQ1	1.2
A24	DDR4_0_DQ10	1.2
B24	DDR4_0_DQ11	1.2
B21	DDR4_0_DQ12	1.2
C23	DDR4_0_DQ13	1.2
D21	DDR4_0_DQ14	1.2
A22	DDR4_0_DQ15	1.2
J19	DDR4_0_DQ16	1.2
M17	DDR4_0_DQ17	1.2
K18	DDR4_0_DQ18	1.2
L19	DDR4_0_DQ19	1.2
B19	DDR4_0_DQ2	1.2
J18	DDR4_0_DQ20	1.2
M16	DDR4_0_DQ21	1.2
J20	DDR4_0_DQ22	1.2
L18	DDR4_0_DQ23	1.2
T22	DDR4_0_DQ24	1.2
R20	DDR4_0_DQ25	1.2
P23	DDR4_0_DQ26	1.2
N23	DDR4_0_DQ27	1.2

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
R22	DDR4_0_DQ28	1.2
P21	DDR4_0_DQ29	1.2
A18	DDR4_0_DQ3	1.2
R21	DDR4_0_DQ30	1.2
P20	DDR4_0_DQ31	1.2
E20	DDR4_0_DQ32	1.2
F18	DDR4_0_DQ33	1.2
F20	DDR4_0_DQ34	1.2
E18	DDR4_0_DQ35	1.2
F19	DDR4_0_DQ36	1.2
G20	DDR4_0_DQ37	1.2
H18	DDR4_0_DQ38	1.2
H17	DDR4_0_DQ39	1.2
A20	DDR4_0_DQ4	1.2
G22	DDR4_0_DQ40	1.2
E23	DDR4_0_DQ41	1.2
G21	DDR4_0_DQ42	1.2
F23	DDR4_0_DQ43	1.2
H24	DDR4_0_DQ44	1.2
E22	DDR4_0_DQ45	1.2
H23	DDR4_0_DQ46	1.2
E21	DDR4_0_DQ47	1.2
J23	DDR4_0_DQ48	1.2
K22	DDR4_0_DQ49	1.2
D18	DDR4_0_DQ5	1.2
K23	DDR4_0_DQ50	1.2
L24	DDR4_0_DQ51	1.2
J24	DDR4_0_DQ52	1.2
L20	DDR4_0_DQ53	1.2
L23	DDR4_0_DQ54	1.2
K20	DDR4_0_DQ55	1.2
P16	DDR4_0_DQ56	1.2
R18	DDR4_0_DQ57	1.2
R17	DDR4_0_DQ58	1.2
N19	DDR4_0_DQ59	1.2
A19	DDR4_0_DQ6	1.2

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
R16	DDR4_0_DQ60	1.2
N18	DDR4_0_DQ61	1.2
N16	DDR4_0_DQ62	1.2
N17	DDR4_0_DQ63	1.2
N14	DDR4_0_DQ64	1.2
R12	DDR4_0_DQ65	1.2
P15	DDR4_0_DQ66	1.2
P14	DDR4_0_DQ67	1.2
M14	DDR4_0_DQ68	1.2
R13	DDR4_0_DQ69	1.2
A17	DDR4_0_DQ7	1.2
L15	DDR4_0_DQ70	1.2
M15	DDR4_0_DQ71	1.2
C21	DDR4_0_DQ8	1.2
D23	DDR4_0_DQ9	1.2
B17	DDR4_0_DQS0_C	1.2
C17	DDR4_0_DQS0_T	1.2
B22	DDR4_0_DQS1_C	1.2
C22	DDR4_0_DQS1_T	1.2
J16	DDR4_0_DQS2_C	1.2
K16	DDR4_0_DQS2_T	1.2
N22	DDR4_0_DQS3_C	1.2
N21	DDR4_0_DQS3_T	1.2
E17	DDR4_0_DQS4_C	1.2
F17	DDR4_0_DQS4_T	1.2
F24	DDR4_0_DQS5_C	1.2
G24	DDR4_0_DQS5_T	1.2
M21	DDR4_0_DQS6_C	1.2
M20	DDR4_0_DQS6_T	1.2
T17	DDR4_0_DQS7_C	1.2
T18	DDR4_0_DQS7_T	1.2
M12	DDR4_0_DQS8_C	1.2
N12	DDR4_0_DQS8_T	1.2
D16	DDR4_0_ODT	1.2
H13	DDR4_0_PAR	1.2
A14	DDR4_0_RESET_N	1.2

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
K15	DDR4_0_TEN	1.2
AG22	DDR4_1_A0	1.2
AE20	DDR4_1_A1	1.2
AH23	DDR4_1_A10	1.2
AH22	DDR4_1_A11	1.2
AF23	DDR4_1_A12	1.2
AF22	DDR4_1_A13	1.2
AK23	DDR4_1_A14	1.2
AE21	DDR4_1_A15	1.2
AL22	DDR4_1_A16	1.2
AF20	DDR4_1_A17	1.2
AL20	DDR4_1_A2	1.2
AJ23	DDR4_1_A3	1.2
AK21	DDR4_1_A4	1.2
AM20	DDR4_1_A5	1.2
AN21	DDR4_1_A6	1.2
AD21	DDR4_1_A7	1.2
AG21	DDR4_1_A8	1.2
AP20	DDR4_1_A9	1.2
AR23	DDR4_1_ACT_N	1.2
AJ20	DDR4_1_ALERT_N	1.2
AK22	DDR4_1_BA0	1.2
AK20	DDR4_1_BA1	1.2
AN23	DDR4_1_BG0	1.2
AE23	DDR4_1_BG1	1.2
AN24	DDR4_1_C0	1.2
AP24	DDR4_1_C1	1.2
AP23	DDR4_1_C2	1.2
AR21	DDR4_1_CK_C	1.2
AP21	DDR4_1_CK_T	1.2
AL23	DDR4_1_CKE	1.2
AR22	DDR4_1_CS_N	1.2
AV24	DDR4_1_DM0	1.2
AV28	DDR4_1_DM1	1.2
AK27	DDR4_1_DM2	1.2
AD25	DDR4_1_DM3	1.2

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AR26	DDR4_1_DM4	1.2
G35	DDR4_1_DM5	1.2
K36	DDR4_1_DM6	1.2
E36	DDR4_1_DM7	1.2
F38	DDR4_1_DM8	1.2
AV23	DDR4_1_DQ0	1.2
AT22	DDR4_1_DQ1	1.2
AR28	DDR4_1_DQ10	1.2
AW25	DDR4_1_DQ11	1.2
AU27	DDR4_1_DQ12	1.2
AV26	DDR4_1_DQ13	1.2
AT28	DDR4_1_DQ14	1.2
AW26	DDR4_1_DQ15	1.2
AL28	DDR4_1_DQ16	1.2
AJ25	DDR4_1_DQ17	1.2
AH26	DDR4_1_DQ18	1.2
AH24	DDR4_1_DQ19	1.2
AT24	DDR4_1_DQ2	1.2
AJ26	DDR4_1_DQ20	1.2
AJ24	DDR4_1_DQ21	1.2
AL27	DDR4_1_DQ22	1.2
AK25	DDR4_1_DQ23	1.2
AD26	DDR4_1_DQ24	1.2
AG27	DDR4_1_DQ25	1.2
AE27	DDR4_1_DQ26	1.2
AF27	DDR4_1_DQ27	1.2
AE26	DDR4_1_DQ28	1.2
AG25	DDR4_1_DQ29	1.2
AT23	DDR4_1_DQ3	1.2
AF25	DDR4_1_DQ30	1.2
AG26	DDR4_1_DQ31	1.2
AM27	DDR4_1_DQ32	1.2
AM24	DDR4_1_DQ33	1.2
AN27	DDR4_1_DQ34	1.2
AN28	DDR4_1_DQ35	1.2
AM26	DDR4_1_DQ36	1.2

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AN26	DDR4_1_DQ37	1.2
AM25	DDR4_1_DQ38	1.2
AP28	DDR4_1_DQ39	1.2
AW23	DDR4_1_DQ4	1.2
H34	DDR4_1_DQ40	1.2
G39	DDR4_1_DQ41	1.2
F37	DDR4_1_DQ42	1.2
G37	DDR4_1_DQ43	1.2
H36	DDR4_1_DQ44	1.2
H39	DDR4_1_DQ45	1.2
G34	DDR4_1_DQ46	1.2
G36	DDR4_1_DQ47	1.2
J38	DDR4_1_DQ48	1.2
J35	DDR4_1_DQ49	1.2
AU22	DDR4_1_DQ5	1.2
K37	DDR4_1_DQ50	1.2
K35	DDR4_1_DQ51	1.2
J39	DDR4_1_DQ52	1.2
J34	DDR4_1_DQ53	1.2
L37	DDR4_1_DQ54	1.2
L35	DDR4_1_DQ55	1.2
E35	DDR4_1_DQ56	1.2
B34	DDR4_1_DQ57	1.2
B36	DDR4_1_DQ58	1.2
D34	DDR4_1_DQ59	1.2
AW21	DDR4_1_DQ6	1.2
D35	DDR4_1_DQ60	1.2
A34	DDR4_1_DQ61	1.2
C36	DDR4_1_DQ62	1.2
C34	DDR4_1_DQ63	1.2
A38	DDR4_1_DQ64	1.2
D38	DDR4_1_DQ65	1.2
C39	DDR4_1_DQ66	1.2
D39	DDR4_1_DQ67	1.2
A37	DDR4_1_DQ68	1.2
E37	DDR4_1_DQ69	1.2

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AV21	DDR4_1_DQ7	1.2
B37	DDR4_1_DQ70	1.2
C37	DDR4_1_DQ71	1.2
AT27	DDR4_1_DQ8	1.2
AV27	DDR4_1_DQ9	1.2
AV22	DDR4_1_DQS0_C	1.2
AU21	DDR4_1_DQS0_T	1.2
AU26	DDR4_1_DQS1_C	1.2
AU25	DDR4_1_DQS1_T	1.2
AL25	DDR4_1_DQS2_C	1.2
AL24	DDR4_1_DQS2_T	1.2
AG24	DDR4_1_DQS3_C	1.2
AF24	DDR4_1_DQS3_T	1.2
AR25	DDR4_1_DQS4_C	1.2
AP25	DDR4_1_DQS4_T	1.2
H38	DDR4_1_DQS5_C	1.2
H37	DDR4_1_DQS5_T	1.2
K38	DDR4_1_DQS6_C	1.2
L38	DDR4_1_DQS6_T	1.2
A35	DDR4_1_DQS7_C	1.2
B35	DDR4_1_DQS7_T	1.2
B39	DDR4_1_DQS8_C	1.2
C38	DDR4_1_DQS8_T	1.2
AE22	DDR4_1_ODT	1.2
AG20	DDR4_1_PAR	1.2
AJ21	DDR4_1_RESET_N	1.2
AD20	DDR4_1_TEN	1.2
AF11	DONE_1V8	1.8
AL33	DXEN	1.8
AE30	DY	1.8
AH31	DZ	1.8
AD14	EMCCLK_B	1.8
AF30	EN_485/EN_232_L	1.8
D9	EXT_CLK_N	MGT_CLK
D10	EXT_CLK_P	MGT_CLK
AM19	FABRIC_CLK	3.3V use LVCMOS33

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AK33	FB	1.8
AJ33	FEN	1.8
AL17	FIREFLY0_INT_L	3.3
AH17	FIREFLY0_MODPRS_L	3.3
AL18	FIREFLY0_RESET_L	3.3
H1	FIREFLY0_RX0_N	MGT
H2	FIREFLY0_RX0_P	MGT
G3	FIREFLY0_RX1_N	MGT
G4	FIREFLY0_RX1_P	MGT
F1	FIREFLY0_RX2_N	MGT
F2	FIREFLY0_RX2_P	MGT
E3	FIREFLY0_RX3_N	MGT
E4	FIREFLY0_RX3_P	MGT
AP19	FIREFLY0_SCL	3.3
AK18	FIREFLY0_SDA	3.3
AK17	FIREFLY0_SEL_L	3.3
H5	FIREFLY0_TX0_N	MGT
H6	FIREFLY0_TX0_P	MGT
G7	FIREFLY0_TX1_N	MGT
G8	FIREFLY0_TX1_P	MGT
F5	FIREFLY0_TX2_N	MGT
F6	FIREFLY0_TX2_P	MGT
E7	FIREFLY0_TX3_N	MGT
E8	FIREFLY0_TX3_P	MGT
AM17	FIREFLY1_INT_L	3.3
AL19	FIREFLY1_MODPRS_L	3.3
AK16	FIREFLY1_RESET_L	3.3
D1	FIREFLY1_RX0_N	MGT
D2	FIREFLY1_RX0_P	MGT
C3	FIREFLY1_RX1_N	MGT
C4	FIREFLY1_RX1_P	MGT
B1	FIREFLY1_RX2_N	MGT
B2	FIREFLY1_RX2_P	MGT
A3	FIREFLY1_RX3_N	MGT
A4	FIREFLY1_RX3_P	MGT
AJ16	FIREFLY1_SCL	3.3

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AH16	FIREFLY1_SDA	3.3
AN16	FIREFLY1_SEL_L	3.3
D5	FIREFLY1_TX0_N	MGT
D6	FIREFLY1_TX0_P	MGT
C7	FIREFLY1_TX1_N	MGT
C8	FIREFLY1_TX1_P	MGT
B5	FIREFLY1_TX2_N	MGT
B6	FIREFLY1_TX2_P	MGT
A7	FIREFLY1_TX3_N	MGT
A8	FIREFLY1_TX3_P	MGT
AJ15	FLASH_A0	1.8
AK15	FLASH_A1	1.8
AN13	FLASH_A10	1.8
AN12	FLASH_A11	1.8
AP14	FLASH_A12	1.8
AP13	FLASH_A13	1.8
AR12	FLASH_A14	1.8
AT12	FLASH_A15	1.8
AP15	FLASH_A16	1.8
AR15	FLASH_A17	1.8
AR13	FLASH_A18	1.8
AT13	FLASH_A19	1.8
AH14	FLASH_A2	1.8
AT14	FLASH_A20	1.8
AU14	FLASH_A21	1.8
AU12	FLASH_A22	1.8
AV12	FLASH_A23	1.8
AV14	FLASH_A24	1.8
AW14	FLASH_A25	1.8
AJ14	FLASH_A3	1.8
AL14	FLASH_A4	1.8
AL13	FLASH_A5	1.8
AL12	FLASH_A6	1.8
AM12	FLASH_A7	1.8
AM14	FLASH_A8	1.8
AN14	FLASH_A9	1.8

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AL15	FLASH_ADV_L	1.8
AB9	FLASH_CE_L	1.8
AE11	FLASH_DQ0	1.8
AD10	FLASH_DQ1	1.8
AG12	FLASH_DQ10	1.8
AH12	FLASH_DQ11	1.8
AK13	FLASH_DQ12	1.8
AK12	FLASH_DQ13	1.8
AH13	FLASH_DQ14	1.8
AJ13	FLASH_DQ15	1.8
AC9	FLASH_DQ2	1.8
AD9	FLASH_DQ3	1.8
AF14	FLASH_DQ4	1.8
AG14	FLASH_DQ5	1.8
AE13	FLASH_DQ6	1.8
AF13	FLASH_DQ7	1.8
AF15	FLASH_DQ8	1.8
AG15	FLASH_DQ9	1.8
AV16	FLASH_OE_L	1.8
AE28	FLASH_WAIT	1.8
AW16	FLASH_WE_L	1.8
AP18	FPGA_CPLD_SPARE	3.3
AF28	FPGA_FLASH_RST_L	1.8
AN31	GP0_1V8_N	1.8
AM31	GP0_1V8_P	1.8
AM29	GP1_1V8_N	1.8 (NC by default)
AL29	GP1_1V8_P	1.8 (NC by default)
AE7	GTH_CLK_0_PIN_N	MGT_CLK
AE8	GTH_CLK_0_PIN_P	MGT_CLK
AA7	GTH_CLK_1_PIN_N	MGT_CLK
AA8	GTH_CLK_1_PIN_P	MGT_CLK
F9	GTH_CLK_2_PIN_N	MGT_CLK
F10	GTH_CLK_2_PIN_P	MGT_CLK
AK31	H/F	1.8
R11	INIT_B_1V8	1.8
G15	MEM_CLK_0_PIN_N	1.2 (External Term Provided)

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
G16	MEM_CLK_0_PIN_P	1.2 (External Term Provided)
AN22	MEM_CLK_1_PIN_N	1.2 (External Term Provided)
AM22	MEM_CLK_1_PIN_P	1.2 (External Term Provided)
V9	MODE_0/2	1.8
T9	MODE_0/2	1.8
AE12	ONBRD_CLK_1V8	1.8
AF12	ONBRD_DATA_1V8	1.8
H9	PCIE_REFCLK_1_PIN_N	MGT_CLK
H10	PCIE_REFCLK_1_PIN_P	MGT_CLK
AT9	PCIE_REFCLK_2_PIN_N	MGT_CLK
AT10	PCIE_REFCLK_2_PIN_P	MGT_CLK
AW3	PCIE_RX0_N	MGT
AW4	PCIE_RX0_P	MGT
AV1	PCIE_RX1_N	MGT
AV2	PCIE_RX1_P	MGT
AU3	PCIE_RX2_N	MGT
AU4	PCIE_RX2_P	MGT
AT1	PCIE_RX3_N	MGT
AT2	PCIE_RX3_P	MGT
AR3	PCIE_RX4_N	MGT
AR4	PCIE_RX4_P	MGT
AP1	PCIE_RX5_N	MGT
AP2	PCIE_RX5_P	MGT
AN3	PCIE_RX6_N	MGT
AN4	PCIE_RX6_P	MGT
AM1	PCIE_RX7_N	MGT
AM2	PCIE_RX7_P	MGT
AW7	PCIE_TX0_PIN_N	MGT
AW8	PCIE_TX0_PIN_P	MGT
AV5	PCIE_TX1_PIN_N	MGT
AV6	PCIE_TX1_PIN_P	MGT
AU7	PCIE_TX2_PIN_N	MGT
AU8	PCIE_TX2_PIN_P	MGT
AT5	PCIE_TX3_PIN_N	MGT
AT6	PCIE_TX3_PIN_P	MGT
AR7	PCIE_TX4_PIN_N	MGT

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AR8	PCIE_TX4_PIN_P	MGT
AP5	PCIE_TX5_PIN_N	MGT
AP6	PCIE_TX5_PIN_P	MGT
AN7	PCIE_TX6_PIN_N	MGT
AN8	PCIE_TX6_PIN_P	MGT
AM5	PCIE_TX7_PIN_N	MGT
AM6	PCIE_TX7_PIN_P	MGT
AE15	PERST_1V8_0_L	MGT
AM15	PERST_1V8_1_L	MGT
AU31	POWER9_SCL_1V8	1.8
AV31	POWER9_SDA_1V8	1.8
AL30	PPS_BUF_1V8	1.8
AA9	PROGRAM_B_1V8	1.8
P11	PUDC_B	1.8
AH28	RA	1.8
AH29	RB	1.8
AH32	RXEN_L	1.8
AG3	SFP+_RX0_N	MGT
AG4	SFP+_RX0_P	MGT
AB1	SFP+_RX1_N	MGT
AB2	SFP+_RX1_P	MGT
AG7	SFP+_TX0_N	MGT
AG8	SFP+_TX0_P	MGT
AB5	SFP+_TX1_N	MGT
AB6	SFP+_TX1_P	MGT
AM16	SFP+0_LOS	3.3
AH19	SFP+0_MOD_ABS	3.3
AJ19	SFP+0_RS0	3.3
AJ18	SFP+0_RS1	3.3
AH18	SFP+0_SCL	3.3
AG16	SFP+0_SDA	3.3
AG17	SFP+0_TX_DISABLE	3.3
AE16	SFP+0_TX_FAULT	3.3
AF17	SFP+1_LOS	3.3
AD18	SFP+1_MOD_ABS	3.3
AD16	SFP+1_RS0	3.3

Table 15 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AE17	SFP+1_RS1	3.3
AE18	SFP+1_SCL	3.3
AF18	SFP+1_SDA	3.3
AF19	SFP+1_TX_DISABLE	3.3
AG19	SFP+1_TX_FAULT	3.3
AU30	SI5328_1V8_SCL	1.8
AU29	SI5328_1V8_SDA	1.8
AN32	SI5328_REFCLK_IN_N	1.8
AM32	SI5328_REFCLK_IN_P	1.8
W7	SI5328_REFCLK_OUT0_PIN_N	MGT_CLK
W8	SI5328_REFCLK_OUT0_PIN_P	MGT_CLK
K9	SI5328_REFCLK_OUT1_PIN_N	MGT_CLK
K10	SI5328_REFCLK_OUT1_PIN_P	MGT_CLK
AR20	SPARE_SCL	3.3
AT20	SPARE_SDA	3.3
AP16	SPARE_WP	3.3
AW19	SRVC_MD_L	3.3
AJ29	TE485	1.8
AT19	USER_LED_G0	3.3
AU19	USER_LED_G1	3.3
AU20	USER_LED_R	3.3
AV18	USR_SW	3.3

Table 15 : Complete Pinout Table

Revision History

Date	Revision	Changed By	Nature of Change
25 Feb 2016	0.1	K. Roth	Initial Draft
29 Mar 2016	1.0	K. Roth	Initial Release, updated Fabric Clock to CMOS, updated photos, updated SDK reference.
4 May 2016	1.1	K. Roth	Updated DDR4 SDRAM to specify DDR4-2133 as maximum speed while include DBI feature as required and added IP core setup list, updated Configuration From Flash Memory by adding Vivado hardware manager setup list, corrected LED Details.
6 Jun 2016	1.2	K. Roth	Added Building and Programming Configuration Images, Removed section: Configuration From Flash Memory, Updated LED figure in LEDs
6 Jan 2017	1.3	K. Roth	Added available power by rail table to Power Requirements, Added section: Custom Flash Write Interface, Updated Firefly part numbers in FireFly, Added note about PCIe RX equalization options.
7 Feb 2017	1.4	K. Roth	Removed references to automatic temperature monitoring and protection.
7 Mar 2017	1.5	K. Roth	Corrected firefly clock speed in Clock Topology, Added scaling factor note regarding current measurement results in System Monitor.
1 May 2017	1.6	K. Roth	VCC_BRAM removed from 1.8V row of table in Power Requirements, Scaled thermal performance graph to match innacuracies of current measurement circuit Thermal Performance, corrected SFP0 and SFP1 location shown in section SFP+, added MIG IP setup requirements rev2 + newer PCBs, updated USB Front Panel Interface to include avr2util instructions.
21 Jun 2017	1.7	K. Roth	Updated all reference to DDR4 speeds at 8G to be 2400MT/s and 16g to be 1866MT/s.
28 Jun 2017	1.8	D. Flint	Updated Thermal Performance with results from more accurate thermal tests.
18 Sep 2017	1.9	K. Roth	Updated Switches for PCIe I2C isolation function added at rev4 PCB, Clocking updated with maximum programable frequency of 312.5MHz, Updated DDR4 SDRAM timing number summary for the custom csv files, updated SFP+ to state that the Si5328 is not fitted only on rev3 and earlier.
20 Dec 2018	1.10	K. Roth	Updated SFP+ details on Si5328, updated GPIO to clarify that the direct connect signals may always be used.

Date	Revision	Changed By	Nature of Change
24 Oct 2019	1.11	K. Roth	Updated USB Front Panel Interface to include clock indexes
14 Jan 2022	1.12	K. Roth	Updated USB Front Panel Interface to correct download links.
17 Jul 2023	1.13	K. Roth	Added Mechanical Dimensions (PCB only)

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